Amendments to the Specification:

Please replace the paragraph on page 9, lines 2-3, with the following paragraph:

Fig. 1 shows an embodiment of an integrated circuit having a synchronous circuit and an asynchronous circuit; ~~and~~

Please replace the paragraph on page 9, lines 5-6, with the following paragraph:

Fig. 2 shows a timing diagram of signals of the integrated circuit shown in Fig. 1[[.]]; and

Please add the following new paragraph after the paragraph on page 9, lines 5-6:

Fig. 3 shows a diagram of the structure of the sequence controller shown in Fig. 1.

Please replace the paragraph on page 10, line 20, to page 11, line 18, with the following paragraph:

Fig. 2 shows a timing diagram of the circuit shown in Fig. 1. The data DA1 are formed by the input data A, B, C and D. At

the beginning of the data transfer from the synchronous circuit 2 into the asynchronous circuit 3, the switch 7 shown in Fig. 1 is closed. In order to transfer the data DA1 in the form of the input data B from the synchronous circuit 2 into the input register circuit 4, the control clock signal C1 has an active state (active high) at the instant t1. The input data B are stored in the input register circuit 4 as data D4. If the sequence controller 6 recognizes from the input data B, for example from a command, that the data processing in the asynchronous circuit will take a comparatively long time, it switches off the control clock signal C1 for the input register circuit 4. To that end, the control signal W is put into an active state (active high). The monitoring of the processing data duration of the asynchronous circuit is performed by the monitoring circuit 61 as shown in Fig. 3. The control signal W is set to an active or inactive state by the W-signal generation circuit 62. The consequence of this is that, in contrast to the clock period P1, in the clock period P2, no input data are transferred into the input register circuit 4. The "old" data D4 are still stored in the input register circuit 4 in order to be processed by the asynchronous circuit 3. To that end, the data D4 are transferred from the input register circuit 4 into the asynchronous circuit 3 and processed in the latter. On account of the control signal W, the control clock signal C1 is

deactivated within the data processing duration TD of the asynchronous circuit 3.

Please replace the paragraph on page 11, line 20, to page 12, line 4, with the following paragraph:

Once the data have been completely processed in the asynchronous circuit 3, a clock pulse is generated in the form of the control clock signal C2 for the output register circuit 5. This operation is performed by the monitoring circuit 61 as shown in Fig. 3. If the monitoring circuit 61 detects that the data in the asynchronous circuit 3 are completely processed, it switches on the switch 63. As a result, the clock pulse CK is transferred in the form of the clock signal C2 to the output register circuit 5. In addition, the signal W is switched back into its inactive state. The control clock signal C2 can be activated at or after the end of the data processing duration TD of the asynchronous circuit 3 (instant t2). The data DA2 are transferred in the form of the processed output data E into the output register circuit 5 and stored (data D5). From the instant t2, the output data E are valid for further processing in the synchronous circuit 2.

Amendment to the drawings:

The attached sheets of drawings include relabeled drawing pages 1/3 - 3/3. Fig. 3 is added as required by the Examiner to further show the structure of the sequence controller.

Attachment: Replacement Sheets